

04/30/2002

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LSI LOGIC-IP DEPT./4084337460 → 9170374672

NO. 483 D004

PTO/SB/08A (10-98)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Sheet

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of

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Complete If Known

Application Number	10/015,194
Filing Date	November-20, 2001
First Named Inventor	Jam s S. Koford
Group Art Unit	2104-212
Examiner Name	
Attorney Docket No.	/01-390

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where	T
AAB		Simplify Programmable-Logic-IP Integration - Author(s) - Cravotta, Robert	
AWP		Altera Casts Spotlight On IP Integration Tool - Author(s) - Souza, Crista	

Examiner signature

ALBERT W. PALADRIN
PATENT EXAMINER

Date considered

6-7-05

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Complete If Known

Application Number	10/015,194
Filing Date	November 20, 2001
First Named Inventor	James S. Koford
Group Art Unit	2184 212
Examiner Name	
Attorney Docket No.	/01-390

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	U.S. Patent Document Number Kind Code (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
Clif		5,222,030	Dangelo et al.	06-22-1993	
Clif		6,574,778	Chang et al.	06-03-2003	

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where	T
Clif		"Rapid Chip Management System"; Filed November 20, 2002; US Serial #10/301,182 - Author(s) - DANIEL M. WEBB	

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ALBERT W. PALACIO
PATENT EXAMINERDate
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LSI GIC-IP DEPT./4084337460 → 9170374619

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Application Number	10/015,194
Filing Date	November-20, 2001
First Named Inventor	James S. Koford
Group Art Unit	-2184 2125
Examiner Name	
Attorney Docket No.	/01-390

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	U.S. Patent Document Number	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Page, Column, Line, Where Relevant Passages or Relevant Figures Appear
AVM		5,553,002	Dangelo et al.	09-03-1996	

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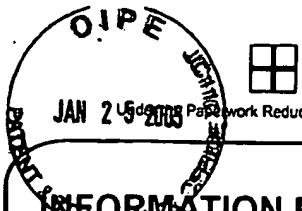
*Albert W. Paladino*ALBERT W. PALADINO
PATENT EXAMINERDate
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Group Art Unit	2184 2125
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Attorney Docket No.	/01-390

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	U.S. Patent Document Number	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
ANP		5,553,002	Dangelo et al.	09-03-1996	
ANP		6,678,875	Pajak et al.	01-13-2004	
GVR		6,721,922	Walters et al.	04-13-2004	
AMV		6,742,165	Lev et al.	05-25-2004	
AMV		2003009724	Koford et al.	05-22-2003	
AMV		2004002511	Chris Hamlin	02-05-2004	
QJM		6,634,008	Dole	10-14-2003	
AMV		6,704,917	Curran et al.	03-09-2004	
AMV		6,269,467	Cheung; Cyrus C. (Hercules,	06-10-2003	
AMV		6,253,358	Shuji Takahashi	06-26-2001	

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where	T
AMV		"A rule based VLSI process flow validation system with macroscopic process simulation", IEEE Transactions on semiconductor manufacturing, vol. 3, no. 4, November 1990, pages 239-246 - Author(s) - Funakoshi et al.	

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ALBERT W. PALACIOS
PATENT EXAMINER

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